Claim Amendments

1-29. (Canceled).

30 (Previously Presented): A method comprising

determining that data has an uncorrectable error, and

generating an error correction and detection code that comprises the data and a plurality of check bits such that the error correction and detection code indicates the uncorrectable error in the data regardless of a later introduced single bit error in the error correction and detection code.

31. (Previously Presented): The method of claim 30 wherein generating the error correction and detection code comprises generating the error correction and detection code such that a receiving device can correct single bit errors, detect double bit errors, detect triple bit errors, and detect quadruple bit errors.

32. (Previously Presented): The method of claim 31 wherein generating the error correction and detection code comprises injecting a triple bit error into the error correction and detection code.

33. (Previously Presented): The method of claim 32 wherein injecting comprises injecting the triple bit error into a nibble of the error correction and detection code.

34. (Previously Presented): The method of claim 30 wherein generating the error correction and detection code comprises generating the error correction detection code such that a device, based upon the error correction and detection code, can correct up

to a X bit error in the error correction and detection code and can detect up to a Y bit error in the error correction and detection code, where Y is greater than or equal to X+3.

35. (Previously Presented): The method of claim 34 wherein generating the error correction and detection code comprises injecting a Z bit error into the error correction and detection code, where Z is greater than X+1 and less than Y.

36. (Previously Presented): A method comprising

generating a code comprising data and a plurality of check bits such that a device, based upon the code, can correct up to a X bit error in the code and can detect up to a Y bit error in the code, where Y is greater than or equal to X+3, and

injecting a Z bit error into the code in response to an uncorrectable error, wherein Z is greater than X+1 and less than Y.

37. (Previously Presented): The method of claim 36 wherein X equals 1, Y equals 4, and Z equals 3.

38. (Previously Presented): The method of claim 36 wherein injecting comprises injecting a triple bit error into a nibble of the code.

39. (Previously Presented): An apparatus comprising

a code generator to generate a code comprising data and a plurality of check bits that a device, based upon the code, can correct up to a X bit error in the code and can detect up to a Y bit error in the code, and

an error injector to inject a Z bit error into the code in response to an uncorrectable error, wherein Z is greater than X+1 and less than Y.

40. (Previously Presented): The apparatus of claim 39 comprising a controller to receive an error status of the data and to cause the error injector to inject the Z bit error in response to the error status indicating an uncorrectable error.

41. (Previously Presented): The apparatus of claim 39 wherein X equals 1, Y equals 4, and Z equals 3.

42. (Previously Presented): The apparatus of claim 39 wherein the error injector injects a triple bit error into a nibble of the code in response to the uncorrectable error.

43. (Previously Presented): A machine-readable medium comprising a plurality of instructions that in response to being executed result in a device,

determining whether data has an uncorrectable error,

generating a code comprising data and a plurality of check bits such that another device, based upon the code, can correct up to a X bit error in the code and can detect up to a Y bit error in the code, and

injecting a Z bit error into the code in response to determining that the data comprises has the uncorrectable error, wherein Z is greater than X+1 and less than Y.

44. (Previously Presented): The machine-readable medium of claim 43 wherein executing the plurality of instructions further result in the device

generating the code such that the another device can correct up to a single bit error and can detect up to a quadruple bit error, and

injecting a triple bit error into the code in response to determining that the data has the uncorrectable error.

45. (Previously Presented): The machine-readable medium of claim 43 wherein executing the plurality of instructions further result in the device injecting a triple bit error into a nibble of the code.

46. (Previously Presented): A system comprising

a receiving device to receive a code, to correct up to a X bit error of the code, to detect up to a Y bit error of the code, and to detect an uncorrectable error of the code in response to detecting that the code comprises greater than a X bit error, and

a transmitting device to transmit the code such that the code comprises data, a plurality of check bits, and a Z bit error in response to the data having the uncorrectable error, where Z is greater than X+1 and less than Y.

47. (Previously Presented): The system of claim 46 wherein X equals 1, Y equals 4, and Z equals 3.

48. (Previously Presented): The system of claim 46 wherein the transmitting device injects a triple bit error into the code prior to transmitting the code.

49. (Currently Amended): The system of claim 46 wherein the transmitting device injects a triple bit error into a nibble of the ~~cod~~ code prior to transmitting the code.